12-26-01 10/018867

PCT

Practitioner's Docket No. UDL 2 0016

CHAPTER II

Preliminary Classification:

Proposed Class:

Subclass:

NOTE: "All applicants are requested to include a preliminary classification on newly filed patent applications. The preliminary classification, preferably class and subclass designations, should be identified in the upper right-hand corner of the letter of transmittal accompanying the application papers, for example 'Proposed Class 2, subclass 129.'" M.P.E.P., § 601, 7th ed.

TRANSMITTAL LETTER TO THE UNITED STATES ELECTED OFFICE (EO/US) (ENTRY INTO U.S. NATIONAL PHASE UNDER CHAPTER II)

PCT/GB00/02256	21 June 2000 (21.06.2000)	21 June 1999 (21.06.1999)
INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED

METHOD OF MODIFYING AN INTEGRATED CIRCUIT
TITLE OF INVENTION

REGAN, Timothy, James
APPLICANT(S)

Box PCT
Assistant Commissioner for Patents
Washington D.C. 20231
ATTENTION: EO/US

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*
*(When using Express Mail, the Express Mail label number is **mandatory**; Express Mail certification is optional.)*

I hereby certify that, on the date shown below, this correspondence is being:

MAILING

■ deposited with the United States Postal Service in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

37 C.F.R. § 1.8(a)

☐ with sufficient postage as first class mail.

37 C.F.R. § 1.10 *

■ as "Express Mail Post Office to Addressee"
Mailing Label No. EL852682099US **(mandatory)**

TRANSMISSION

☐ facsimile transmitted to the Patent and Trademark Office, (703) ____-____

Karen Forsyth
Signature

Date: 12/19/01

Karen M. Forsyth
(type or print name of person certifying)

** Only the date of filing (§ 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under § 1.8 continues to be taken into account in determining timeliness. See § 1.703(f). Consider "Express Mail Post Office to Addressee" (§ 1.10) or facsimile transmission (§ 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

NOTE: To avoid abandonment of the application, the applicant shall furnish to the USPTO, not later than 20 months from the priority date: (1) a copy of the international application, unless it has been previously communicated by the International Bureau or unless it was originally filed in the USPTO; and (2) the basic national fee (see 37 C.F.R. § 1.492(a)). The 30-month time limit may not be extended. 37 C.F.R. § 1.495.

WARNING: *Where the items are those which can be submitted to complete the entry of the international application into the national phase are subsequent to 30 months from the priority date the application is still considered to be in the international state and if mailing procedures are utilized to obtain a date the express mail procedure of 37 C.F.R. § 1.10 must be used (since international application papers are not covered by an ordinary certificate of mailing—See 37 C.F.R. § 1.8.*

NOTE: Documents and fees must be clearly identified as a submission to enter the national state under 35 U.S.C. § 371 otherwise the submission will be considered as being made under 35 U.S.C. § 111. 37 C.F.R. § 1.494(f).

I. Applicant herewith submits to the United States Elected Office (EO/US) the following items under 35 U.S.C. § 371:

a. ☒ This express request to immediately begin national examination procedures (35 U.S.C. § 371(f)).

b. ☒ The U.S. National Fee (35 U.S.C. § 371(c)(1)) and other fees (37 C.F.R. § 1.492) as indicated below:

2. Fees

CLAIMS FEE	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
☐*	TOTAL CLAIMS	18 −20=	0	× $18.00=	$ .00
	INDEPENDENT CLAIMS	1 −3=	0	× $84.00=	.00
	MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	
BASIC FEE**	■ U.S. PTO WAS INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where an International preliminary examination fee as set forth in § 1.482 has been paid on the international application to the U.S. PTO: ☐ and the international preliminary examination report states that the criteria of novelty, inventive step (non-obviousness) and industrial activity, as defined in PCT Article 33(1) to (4) have been satisfied for all the claims presented in the application entering the national stage (37 C.F.R. § 1.492(a)(4)) ..... $100.00 ☐ and the above requirements are not met (37 C.F.R. § 1.492(a)(1)) ..... $710.00 ■ U.S. PTO WAS NOT INTERNATIONAL PRELIMINARY EXAMINATION AUTHORITY Where no international preliminary examination fee as set forth in § 1.482 has been paid to the U.S. PTO, and payment of an international search fee as set forth in § 1.445(a)(2) to the U.S. PTO: ☐ has been paid (37 C.F.R. § 1.492(a)(2)) ..... $740.00 ☐ has not been paid (37 C.F.R. § 1.492(a)(3)) ..... $1040.00 ■ where a search report on the international application has been prepared by the European Patent Office or the Japanese Patent Office (37 C.F.R. § 1.492(a)(5)) $890.00				890.00
	Total of above Calculations				= 890.00
SMALL ENTITY	Reduction by 1/2 for filing by small entity, if applicable. Assertion must be made. (note 37 C.F.R. § 1.27)				− 445.00
	Subtotal				445.00
	Total National Fee				$
	Fee for recording the enclosed assignment document $40.00 (37 C.F.R. § 1.21(h)). (See Item 13 below). See attached "ASSIGNMENT COVER SHEET".				
TOTAL	Total Fees enclosed				$ 445.00

*See attached Preliminary Amendment Reducing the Number of Claims.

☒ Attached is a ☒ check ☐ money order in the amount of $ 445.00

☒ Authorization is hereby made to charge the amount of $ _____

☒ to Deposit Account No. 06-0308

☐ to Credit card as shown on the attached credit card information authorization form PTO-2038.

WARNING: *Credit card information should* ***not*** *be included on this form as it may become public.*

☒ Charge any additional fees required by this paper or credit any overpayment in the manner authorized above.

A duplicate of this paper is attached.

"WARNING: *"To avoid abandonment of the application the applicant shall furnish to the United States Patent and Trademark Office not later than the expiration of 30 months from the priority date: * * * (2) the basic national fee (see § 1.492(a)). The 30-month time limit may not be extended." 37 C.F.R. § 1.495(b).*

WARNING: *If the translation of the international application and/or the oath or declaration have not been submitted by the applicant within thirty (30) months from the priority date, such requirements may be met within a time period set by the Office. 37 C.F.R. § 1.495(b)(2). The payment of the surcharge set forth in § 1.492(e) is required as a condition for accepting the oath or declaration later than thirty (30) months after the priority date. The payment of the processing fee set forth in § 1.492(f) is required for acceptance of an English translation later than thirty (30) months after the priority date. Failure to comply with these requirements will result in abandonment of the application. The provisions of § 1.136 apply to the period which is set. Notice of Jan. 3, 1993, 1147 O.G. 29 to 40.*

☒ **Assertion of Small Entity Status**

☒ **Applicant hereby asserts status as a small entity under 37 C.F.R. § 1.27.**

NOTE: 37 C.F.R. § 1.27(c) deals with the assertion of small entity status, whether by a written specific declaration thereof or by payment as a small entity of the basic filing fee or the fee for the entry into the national phase as states:

"(c) Assertion of small entity status. Any party (person, small business concern or nonprofit organization) should make a determination, pursuant to paragraph (f) of this section, of entitlement to be accorded small entity status based on the definitions set forth in paragraph (a) of this section, and must, in order to establish small entity status for the purpose of paying small entity fees, actually make an assertion of entitlement to small entity status, in the manner set forth in paragraphs (c)(1) or (c)(3) of this section, in the application or patent in which such small entity fees are to be paid.

(1) Assertion by writing. Small entity status may be established by a written assertion of entitlement to small entity status. A written assertion must:

(i) Be clearly identifiable;

(ii) Be signed (see paragraph (c)(2) of this section); and

(iii) Convey the concept of entitlement to small entity status, such as by stating that applicant is a small entity, or that small entity status is entitled to be asserted for the application or patent. While no specific words or wording are required to assert small entity status, the intent to assert small entity status must be clearly indicated in order to comply with the assertion requirement.

(2) Parties who can sign and file the written assertion. The written assertion can be signed by:

(i) One of the parties identified in §§ 1.33(b) (e.g., an attorney or agent registered with the Office), §§ 3.73(b) of this chapter notwithstanding, who can also file the written assertion;

(ii) At least one of the individuals identified as an inventor (even though a §§ 1.63 executed oath or declaration has not been submitted), notwithstanding §§ 1.33(b)(4), who can also file the written assertion pursuant to the exception under §§ 1.33(b) of this part; or

(iii) An assignee of an undivided part interest, notwithstanding §§ 1.33(b)(3) and 3.73(b) of this chapter, but the partial assignee cannot file the assertion without resort to a party identified under §§ 1.33(b) of this part.

(3) Assertion by payment of the small entity basic filing or basic national fee. The payment, by any party, of the exact amount of one of the small entity basic filing fees set forth in §§ 1.16(a), (f), (g), (h), or (k), or one of the small entity basic national fees set forth in §§ 1.492(a)(1), (a)(2), (a)(3), (a)(4), or (a)(5), will be treated as a written assertion of entitlement to small entity status even if the type of basic filing or basic national fee is inadvertently selected in error.

(i) If the Office accords small entity status based on payment of a small entity basic filing or basic national fee under paragraph (c)(3) of this section that is not applicable to that application, any balance of the small entity fee that is applicable to that application will be due along with the appropriate surcharge set forth in §§ 1.16(e), or §§ 1.16(l).

(ii) The payment of any small entity fee other than those set forth in paragraph (c)(3) of this section (whether in the exact fee amount or not) will not be treated as a written assertion of entitlement to small entity status and will not be sufficient to establish small entity status in an application or a patent."

3. ☒ A copy of the International application as filed (35 U.S.C. § 371(c)(2)):

NOTE: Section 1.495 (b) was amended to require that the basic national fee and a copy of the international application must be filed with the Office by 30 months from the priority date to avoid abandonment. "The International Bureau normally provides the copy of the international application to the Office in accordance with PCT Article 20. At the same time, the International Bureau notifies applicant of the communication to the Office. In accordance with PCT Rule 47.1, that notice shall be accepted by all designated offices as conclusive evidence that the communication has duly taken place. Thus, if the applicant desires to enter the national stage, the applicant normally need only check to be sure the notice from the International Bureau has been received and then pay the basic national fee by 30 months from the priority date." Notice of Jan. 7, 1993, 1147 O.G. 29 to 40, at 35-36. See item 14c below.

a. ☐ is transmitted herewith.

b. ☐ is not required, as the application was filed with the United States Receiving Office.

c. ☒ has been transmitted

i. ☒ by the International Bureau.

Date of mailing of the application (from form PCT/1B/308): 28 December 2000

ii. ☐ by applicant on ______________. *(Date)*

4. ☒ A translation of the International application into the English language (35 U.S.C. § 371(c)(2)):

a. ☐ is transmitted herewith.

b. ☒ is not required as the application was filed in English.

c. ☐ was previously transmitted by applicant on __________. *(Date)*

d. ☐ will follow.

5. ☒ Amendments to the claims of the International application under PCT Article 19 (35 U.S.C. § 371(c)(3)):

NOTE: The Notice of January 7, 1993 points out that 37 C.F.R. § 1.495(a) was amended to clarify the existing and continuing practice that PCT Article 19 amendments must be submitted by 30 months from the priority date and this deadline may not be extended. The Notice further advises that: "The failure to do so will not result in loss of the subject matter of the PCT Article 19 amendments. Applicant may submit that subject matter in a preliminary amendment filed under section 1.121. In many cases, filing an amendment under section 1.121 is preferable since grammatical or idiomatic errors may be corrected." 1147 O.G. 29-40, at 36.

a. ☐ are transmitted herewith.

b. ☐ have been transmitted

i. ☐ by the International Bureau.

Date of mailing of the amendment (from form PCT/1B/308):

_____.

ii. ☐ by applicant on _____. *(Date)*

c. ☒ have not been transmitted as

i. ☒ applicant chose not to make amendments under PCT Article 19. Date of mailing of Search Report (from form PCT/ISA/210.):

12 October 2000

ii. ☐ the time limit for the submission of amendments has not yet expired. The amendments or a statement that amendments have not been made will be transmitted before the expiration of the time limit under PCT Rule 46.1.

6. ☒ A translation of the amendments to the claims under PCT Article 19 (38 U.S.C. § 371(c)(3)):

a. ☐ is transmitted herewith.

b. ☐ is not required as the amendments were made in the English language.

c. ☒ has not been transmitted for reasons indicated at point 5(c) above.

7. ☒ A copy of the international examination report (PCT/IPEA/409)

☒ is transmitted herewith.

☐ is not required as the application was filed with the United States Receiving Office.

8. ☒ Annex(es) to the international preliminary examination report

a. ☒ is/are transmitted herewith.

b. ☐ is/are not required as the application was filed with the United States Receiving Office.

9. ☒ A translation of the annexes to the international preliminary examination report

a. ☐ is transmitted herewith.

b. ☒ is not required as the annexes are in the English language.

10. ☒ An oath or declaration of the inventor (35 U.S.C. § 371(c)(4)) complying with 35 U.S.C. § 115

a. ☐ was previously submitted by applicant on _____. *(Date)*

b. ☐ is submitted herewith, and such oath or declaration

i. ☐ is attached to the application.

ii. ☐ identifies the application and any amendments under PCT Article 19 that were transmitted as stated in points 3(b) or 3(c) and 5(b); and states that they were reviewed by the inventor as required by 37 C.F.R. § 1.70.

c. ☒ will follow.

II. Other document(s) or information included:

11. ☒ An International Search Report (PCT/ISA/210) or Declaration under PCT Article 17(2)(a):

a. ☒ is transmitted herewith.

b. ☐ has been transmitted by the International Bureau.

Date of mailing (from form PCT/IB/308): _____.

c. ☐ is not required, as the application was searched by the United States International Searching Authority.

d. ☐ will be transmitted promptly upon request.

e. ☐ has been submitted by applicant on _____. *(Date)*

12. ☒ An Information Disclosure Statement under 37 C.F.R. §§ 1.97 and 1.98:

a. ☐ is transmitted herewith.

Also transmitted herewith is/are:

☐ Form PTO-1449 (PTO/SB/08A and 08B).

☐ Copies of citations listed.

b. ☒ will be transmitted within THREE MONTHS of the date of submission of requirements under 35 U.S.C. § 371(c).

c. ☐ was previously submitted by applicant on _____. *(Date)*

13. ☐ An assignment document is transmitted herewith for recording.

A separate ☐ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☐ FORM PTO 1595 is also attached.

_____

_____

_____

14. ☒ Additional documents:
   a. ☐ Copy of request (PCT/RO/101)
   b. ☒ International Publication No. WO 00/79595 A1
      i. ☐ Specification, claims and drawing
      ii. ☐ Front page only
   c. ☒ Preliminary amendment (37 C.F.R. § 1.121)
   d. ☐ Other

____
____
____

15. ☒ The above checked items are being transmitted
   a. ☒ before 30 months from any claimed priority date.
   b. ☐ after 30 months.

16. ☐ Certain requirements under 35 U.S.C. § 371 were previously submitted by the applicant on __________, namely:

____
____
____
____
____

AUTHORIZATION TO CHARGE ADDITIONAL FEES

WARNING: *Accurately count claims, especially multiple dependant claims, to avoid unexpected high charges if extra claims are authorized.*

NOTE: "A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. An authorization to charge all required fees, fees under § 1.17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission. Submission of the fee set forth in § 1.17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C.F.R. § 1.136(a)(3).

NOTE: "Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C.F.R. § 1.26(a).

☒ Please charge, in the manner authorized above, the following additional fees that may be required by this paper and during the entire pendency of this application:

☒ 37 C.F.R. § 1.492(a)(1), (2), (3), and (4) (filing fees)

WARNING: *Because failure to pay the national fee within 30 months without extension (37 C.F.R. § 1.495(b)(2)) results in abandonment of the application, it would be best to always check the above box.*

(Transmittal Letter to the United States Elected Office (EO/US) **[13-18]**—page 8 of 9)

☐ 37 C.F.R. § 1.492(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 C.F.R. § 1.492(d)), it might be best not to authorize the PTO to charge additional claim fees, except possible when dealing with amendments after final action.

☒ 37 C.F.R. § 1.17 (application processing fees)

☒ 37 C.F.R. § 1.17(a)(1)–(5) (extension fees pursuant to § 1.136(a).

☐ 37 C.F.R. § 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. § 1.311(b))

NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 C.F.R. § 1.311(b).

NOTE: 37 C.F.R. § 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying . . . issue fee." From the wording of 37 C.F.R. § 1.28(b): (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

☐ 37 C.F.R. § 1.492(e) and (f) (surcharge fees for filing the declaration and/or filing an English translation of an International Application later than 30 months after the priority date).

SIGNATURE OF PRACTITIONER

Reg. No.: 34,261

Mark S. Svat

(type or print name of practitioner)

Tel. No.: (216) 861-5582

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1100 Superior Avenue - 7th Floor

P.O. Address

Customer No.:

Cleveland, OH 44114-2518

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Timothy James REGAN
For	:	METHOD OF MODIFYING AN INTEGRATED CIRCUIT
Int'l Application No.	:	PCT/GB00/02256
Int'l Filing Date	:	June 21, 2000
Group Art Unit	:	Unknown
Examiner	:	Unknown
Attorney Docket No.	:	UDL 2 0016

Cleveland, Ohio 44114-2518
December 19, 2001

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Dear Sir:

Prior to substantive examination of the above-referenced patent application, applicant respectfully requests amendment of the application as follows:

(THE FOLLOWING AMENDMENTS ARE MADE TO THE CLAIMS AS AMENDED BEFORE THE PCT INTERNATIONAL AUTHORITIES. SUBSTITUTE SHEETS SHOWING THE CLAIMS AS PENDING BEFORE ENTRY OF THIS PRELIMINARY AMENDMENT ARE ANNEXED TO THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT (IPER) SUBMITTED HEREWITH)

IN THE CLAIMS:

(WORKING FROM AMENDED SHEETS 26, 27 ANNEXED TO THE IPER)

Kindly substitute amended claims 1, 3-7, 9 and 11-15 for pending claims 1, 3-7, 9 and 11-15, and add new claims 16-18 as follows:

1. (Amended) A method of modifying a data model of an integrated circuit by electronic means, wherein the data model includes at least one layer of circuit components and wherein the method includes the steps of:

selecting a scaling factor,

scaling the entire circuit represented by the data model according to the scaling factor, and

adjusting each layer in the circuit for functionality and design rule compliance.

3. (Amended) A method according to claim 1, wherein the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios.

4. (Amended) A method according to claim 1, wherein the predetermined scaling ratios include the interconnect scaling ratio including geometry width and spacing for each routing layer, the via size ratio in each via layer and the transistor geometry ratio.

5. (Amended) A method according to claim 3, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

6. (Amended) A method according to claim 1, wherein the step of scaling the circuit according to the scaling factor includes multiplying the coordinates of the circuit geometry by the scaling factor.

7. (Amended) A method according to claim 1, wherein the step of adjusting the circuit for functionality and design rule compliance includes a hierarchical layer scaling process whereby shapes in a sub-cell of the circuit may be scaled without breaking their connections with other parts of the circuit.

9. (Amended) A method according to claim 1, wherein the step of adjusting the circuit for functionality and design rule compliance includes a transistor edge adjustment process.

11. (Amended) A method according to claim 1, including the additional step of updating the contacts and vias by removing the existing contacts and vias and replacing them with new contacts and vias so as to reduce the current density through those contacts and vias.

12. (Amended) A method according to claim 1, including the step of adding and/or deleting layers in accordance with the target manufacturing process.

13. (Amended) A method according to claim 1, including the step of checking the circuit using a layout verification process.

14. (Amended) A method according to claim 1, including the preliminary step of analysing and modifying the circuit data.

15. (Amended) A method according to claim 1, including the step of adding a node containing design parameters to devices in the circuit.

16. (New) A method according to claim 2, wherein the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios.

17. (New) A method according to claim 4, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

18. (New) A method according to claim 16, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

Remarks

Applicant respectfully requests that the foregoing amendments be entered prior to substantive examination of the application. These changes are submitted to place the application in better form for examination.

Respectfully submitted,

FAY, SHARPE, FAGAN,
MINNICH & McKEE LLP

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(216) 861-5582

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Kindly amend claims 1, 3-7, 9 and 11-15 and add new claims 16-18 as follows:

1. (Amended) A method of modifying a data model of an integrated circuit by electronic means, wherein the data model includes at least one layer of circuit components and wherein the method includes the steps of:

[-] selecting a scaling factor,

[-] scaling the entire circuit represented by the data model according to the scaling factor, and

[-] adjusting each layer in the circuit for functionality and design rule compliance.

3. (Amended) A method according to claim 1 [or claim 2], wherein the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios.

4. (Amended) A method according to [any one of the preceding claims] claim 1, wherein the predetermined scaling ratios include the interconnect scaling ratio including geometry width and spacing for each routing layer, the via size ratio in each via layer and the transistor geometry ratio.

5. (Amended) A method according to claim 3 [or claim 4], wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

6. (Amended) A method according to [any one of the preceding claims] claim 1, wherein the step of scaling the circuit according to the scaling factor

includes multiplying the coordinates of the circuit geometry by the scaling factor.

7. (Amended) A method according to [any one of the preceding claims] claim 1, wherein the step of adjusting the circuit for functionality and design rule compliance includes a hierarchical layer scaling process whereby shapes in a sub-cell of the circuit may be scaled without breaking their connections with other parts of the circuit.

9. (Amended) A method according to [any one of the preceding claims] claim 1, wherein the step of adjusting the circuit for functionality and design rule compliance includes a transistor edge adjustment process.

11. (Amended) A method according to [any one of the preceding claims] claim 1, including the additional step of updating the contacts and vias by removing the existing contacts and vias and replacing them with new contacts and vias so as to reduce the current density through those contacts and vias.

12. (Amended) A method according to [any one of the preceding claims] claim 1, including the step of adding and/or deleting layers in accordance with the target manufacturing process.

13. (Amended) A method according to [any one of the preceding claims] claim 1, including the step of checking the circuit using a layout verification process.

14. (Amended) A method according to [any one of the preceding claims] claim 1, including the preliminary step of analysing and modifying the circuit data.

15. (Amended) A method according to [any one of the preceding claims] claim 1, including the step of adding a node containing design parameters to devices in the circuit.

16. (New) A method according to claim 2, wherein the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios.

17. (New) A method according to claim 4, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

18. (New) A method according to claim 16, wherein the data model of the integrated circuit includes a design grid and wherein the scaling factor is selected by rounding up to the next whole design grid point from the largest of the predetermined scaling ratios.

17/prts

METHOD OF MODIFYING AN INTEGRATED CIRCUIT

The present invention relates to a method of modifying an integrated circuit, in particular through a series of scaling operations.

In particular, but not exclusively, the invention relates to a process by which the physical design or layout of an integrated circuit or subcircuit can be modified to meet a different set of design and manufacturing rules. This method involves analysing data of the existing integrated circuit to determine the scaling factor then altering the shapes in the original by scaling the data, scaling individual layers, adjusting the edges of shapes and swapping geometries and cells through a defined sequence, according to a process migration technique.

Process migration is a technique for modifying integrated circuit designs so that they can be manufactured by new manufacturing processes with different geometric sizes and relationships. The physical size of an integrated circuits is limited by the manufacturing process used. The limiting factor is the size of the smallest component that can be produced, which at present is approximately 0.13 microns.

As new processes are devised, components can be manufactured to smaller sizes. However, before an existing circuit can be built at a smaller scale using a new manufacturing process, the circuit layout must be re-designed. The overall plan of the circuit may be approximately the same, but different parts and components of the circuit may need to be scaled by differing factors. There are rules governing these critical dimensions. Some rely on manufacturing constraints, for example the smallest feasible size of a connection, whereas others depend on electronic factors such as capacitance and resistance.

When re-designed, computers can check the circuits for compliance with these design rules.

There may be various reasons for switching to a new manufacturing process, including:

1) SPEED: smaller components have faster switching due to smaller charge transfer requirements and smaller signalling distances.

2) SIZE: unit costs are lower, as more chips can be made per silicon wafer

3) ECONOMIC PRODUCTION: more products can be made on one production line, allowing older, less economical, production lines to be closed.

The main problem is how to modify the physical design of the circuit. This can be very difficult and complicated.

Another reason for re-designing the chips is that many circuits are now designed using parts or components supplied by different manufacturers, called "system-on-chip" components. However, these components may be produced by different manufacturers and made to different design rules, and need to be re-designed so that they all comply to the same set of designs rules.

Reasons for re-designing might therefore include:

1) Compliance with particular design rules;

2) To make use of the latest manufacturing processes; and

3) To reduce the size of the component by a certain factor.

Existing methods of process migration are as follows:

Symbolic Migration. In this, each component, such as each transistor, is re-generated according to required technical specifications. The process is not very successful, especially for complicated circuits.

Compaction. It is known, for example from US 5640497, to provide a method of redesigning layouts. In this method, the circuit is made smaller by squeezing all the dimensions to the smallest allowed by the design rules, first in the x direction and then in the y direction. The technique is partially successful, but "flattens" the circuit: i.e. it destroys the hierarchy of the building blocks. This requires huge computing power to achieve and, because the hierarchy can no longer be identified, it makes subsequent modification extremely difficult.

Scaling. Scaling implies reducing the size of each component by a constant factor. While this reduces the size of the component, the resulting circuit will generally be inoperable as it is likely to break many hundreds-of-thousands of design rules. Therefore, while this is sometimes seen as the ideal solution, it has not previously been achievable.

It is an object of the present invention to provide a method of scaling an integrated circuit that mitigates at least some of the aforesaid problems.

According to the present invention there is provided a method of modifying an integrated circuit, the method including the steps of selecting a scaling factor, scaling the circuit according to the scaling factor, and adjusting the circuit for functionality and design rule compliance.

The method makes it possible to scale a circuit without losing functionality or destroying the hierarchy of the circuit.

Advantageously, the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios. This ensures that the circuit is scaled to the maximum degree without violating essential design rules. Advantageously, the predetermined scaling ratios include the interconnect scaling ratio, the via size ratio and the electrical component geometry ratio.

Advantageously, the scaling factor is selected by rounding up to the next whole grid point from the largest of the predetermined scaling ratios. This ensures that the components of the circuit are placed correctly on the design grid.

Advantageously, the step of scaling the circuit according to the scaling factor circuit includes multiplying the co-ordinates of the circuit geometry by the scaling factor.

Advantageously, the step of adjusting the circuit for functionality and design rule compliance includes a hierarchical layer scaling process. The hierarchical layer scaling process may include the step of scaling the components in a layer according to a predetermined layer scaling factor. This may be achieved by absolute scaling (adding or subtracting a fixed amount to the size of each component), or alternatively by relative

scaling (multiplying to increase or decrease the size of each component by a fixed percentage of its original size) . The hierarchical layer scaling process may include the step of scaling the components so as to maintain the connectivity of those components. The hierarchical layer scaling process may include the step of identifying components that meet predetermined width criteria, and scaling only components that do not meet those criteria. In this way, power connectors can be excluded from the scaling process, to avoid overheating problems.

Advantageously, the step of adjusting the circuit for functionality and design rule compliance includes a transistor edge adjustment process. The transistor edge adjustment process may include the step of adjusting the width of the polysilicon layer and/or the length of the diffusion layer. This restores the correct dimensions of the components making up the transistors, to ensure functionality.

Advantageously, the method includes the step of updating the contacts and vias. The step of updating the contacts and vias may include removing the existing contacts and vias and replacing them with new contacts and vias, to reduce current density.

Advantageously, the method includes the step of adding and/or deleting layers, to accommodate changes in technology.

Advantageously, the method includes the step of checking the circuit using a layout verification process to ensure compliance with design rules.

Advantageously, the method includes the preliminary step of analysing and modifying the circuit data, to reduce the time needed to complete the migration process.

Advantageously, the method includes the step of adding nodes containing design parameters to devices in the circuit, so allowing easy access to information about those devices.

It is a further object of the present invention to provide a different process migration technique which may be described as "complex scaling" and which is applicable to the computer model of the layout of any existing integrated circuit. By using this technique,

the layout of a chip may be modified to be manufactured in any new process and at any scale that meets the new design rules.

The method is applicable to flat chip layouts and those containing design hierarchy, which may be defined as the placing of sub-cells into higher level circuits and these, in turn, being placed again. The hierarchy of the migrated chip matches the hierarchy of the original.

According to another aspect of the present invention, there is provided a method of scaling an integrated circuit comprising the steps of examining the existing layout to determine the amount by which the layout must be scaled, including determining variable geometry values; absolute geometry values; and a design grid, and carrying out one or more of gate width and length adjustment; layer scaling; polygon edge adjustment; contact replacement; adjust overlaps; addition or removal of layers; cell swapping; and verification.

An embodiment of the invention will be now be more particularly described by way of example and with reference to the accompanying drawings, in which:

Figure 1 shows circuit hierarchy where building blocks of circuitry are placed into larger blocks which can be placed again into yet larger blocks;

Figure 2 shows variable rule examples, where geometry must be equal to or greater than a set distance and width;

Figure 3 shows fixed geometry value examples, where geometry dimensions must equal a defined value;

Figure 4 shows interconnect spacing;

Figure 5 shows via geometries and arrays;

Figures 6a and 6b show CMOS transistor geometry, and Figure 6c shows spacing considerations in a lateral transistor;

Figures 7a and 7b show general scaling;

Figure 8 shows CMOS transistor definition and transistor edge adjustment;

Figure 9 shows adjusting the gate width of multiple transistors formed on a single diffusion geometry;

Figure 10 is illustrative of layer shrinking breaking connectivity;

Figure 11 illustrates hierarchical layer shrink with connectivity;

Figure 12 shows layer sizing by geometry width;

Figure 13 shows edge adjustment for transistors;

Figure 14 illustrates the use of contacts and vias to connect components of the circuit;

Figure 15 shows contact removal and replacement;

Figure 16 shows layer overlap;

Figure 17 shows a new well defined around an existing diffusion;

Figure 18 shows moving routing data between layers;

Figure 19 shows swapping new via cells for old;

Figure 20 shows the steps of the migration process in the form of a flow diagram;

Figure 21 shows the steps of the layer sizing process as a flow diagram;

Figures 22a, 22b and 22c show nodes placed over a transistor, a resistor and a capacitor;

Figure 23 shows size calculations for a resistor, and

Figures 24a and 24b show size calculations for a capacitor.

A typical circuit hierarchy is shown in figure 1. Building blocks 1 of a circuit are placed into larger blocks 2, which can be placed again into yet larger blocks 3.

The cell migration process consists of three distinct steps:

1) Calculating the ideal scaling factor;

2) Scaling the entire circuit using the calculated factor; and

3) Fixing any errors in the circuit.

These steps are described in more detail below.

In the first step, the ideal scaling factor is calculated using at least three sets of equations, which are described in more detail below with reference to figures 2 to 6. When each of these equations has been solved, the scaling factor used is the smallest allowed by all of the equations. In other words, the end circuit is no smaller than is allowed by all of the equations.

In the second step, the entire circuit is scaled using the calculated factor. This is done by multiplying every dimension by the same factor, which includes the positions of the building blocks, the positions and dimensions of the connectors, the positions of components within building blocks and the geometries of those components.

As shown in figure 7, the end result is a scale copy of the original circuit. However, many design rules will have been violated and component values will be incorrect: e.g. the width and length of the transistors may be too big or too small, giving either slow operation or non-operation. The resistors and capacitors may also have incorrect values.

The third step is to fix the errors. There are various steps to the fixing operation, as follows:

1) The size of all the geometries in any particular layer may be adjusted, by adjusting the layer size. For example, the co-ordinates of the shapes in the polysilicon layer may be adjusted. This is know as "layer sizing". For example, the area of polysilicon over the diffusion making up the transistor may be increased or decreased so as to achieve the minimum dimensions or to provide minimum separations. This is shown in Figures 10-11. The dimensions are changed by a fixed amount (e.g. 0.2 microns) rather than as a percentage of the original shape.

2) Some parts of some components may be left unaltered: in particular power connectors are not reduced in size, as this could affect the current flow in the circuit. The power connectors are identified by their size, as they are often larger than the other connectors, or by their signal name. The control logic therefore keeps components of a particular size unaltered, and reduces the size only of those that fall below a certain limit. This is shown in Figure 12.

3) Edge Adjustment. If the area of a component is too large, or if one edge is too close to another component following layer sizing or scaling, it can be adjusted by

moving one edge of the component rather than by changing the size of the whole component. This is shown in Figure 13. For example, the size of a transistor can be altered in this way.

The scaling process therefore consists of three steps:

1) Overall scaling to a fixed factor;

2) Fixed scaling of components (layer scaling), which may include up to three separate steps; and

3) Edge adjustment.

The process may in addition include the following features, which are preferred but not essential.

1) Contact removal and replacement (see Figure 15) it is desirable to provide as many electrical contacts as possible on each component, so reducing the current density through those contacts. Instead of re-scaling the contacts, it is better simply to remove them and then insert as many contacts as possible in the space available, according to the new design rules.

2) Adding and removing layers (see Figure 17). Some manufacturing processes need more layers than previous ones, and some do not require as many. The process can be modified to add or subtract layers as required. For example, if the new process requires an extra layer to make a transistor, the computer can be arranged to identify each transistor (for example by recognising a layer of polysilicon over a diffusion layer), and then add an extra layer as required.

The process and the steps making up the process will now be described in more detail.

The technique for modifying the circuit involves a series of steps that scale the data and modify the shapes contained within it to comply with a set of design rules that govern the manufacturing process for production of the finished chip.

The techniques contained in this process will work for all components and connection geometries on a chip including, but not restricted to, MOSFET and bipolar transistors, resistors, capacitors and diodes.

The input data for the process migration can be any existing chip or IC layout or the intellectual property contained therein, in an industry standard format such as GDSII or CIF. These files will contain the data that makes up the chip and may include rectangles, polygons, paths, instances, arrays and labels.

A modification sequence will include some or all of the following:-

Design analysis and scaling calculations;

General scaling;

Gate width and length adjustment;

Layer scaling;

Polygon edge adjustment;

Contact replacement;

Adjust overlaps;

Addition or removal of layers;

Cell swapping;

Verification.

In order to apply a factor to the general scaling calculations it is necessary to examine the existing layout to determine the amount by which the layout must be scaled. There are three factors that must be taken into account in this process:-

1. Variable geometry values;
2. Absolute geometry values;
3. The design grid.

Taking the first of these, namely variable geometry values, many of the design rules in an integrated circuit manufacturing process are given as a minimum value and must be met or exceeded when designing the circuit. An example of this would be a rule that determines the spacing between two geometries on the same layer that is enforced to ensure that the two geometries do not merge together during manufacture. The spacing rule may be exceeded as long as the minimum value given is not violated.

Examples of variable geometry values include widths, spacings and enclosures of layers.

Figure 2 shows variable rule examples, where the separation 4, the overlap 5 and the width 6 of different geometries must be equal to or greater than a set distance.

The second factor relates to absolute geometry values. Integrated circuit design rules usually have fixed values for certain geometries that must be met and cannot be exceeded. These are usually applied to contact and via holes that connect routing circuitry and this value must be met for each occurrence of these shapes. In addition, transistor sizes are defined in the circuit net list and this must be matched in the layout. Failure to meet these values will result in errors when checking the layout against the circuit schematic or netlist.

As shown in figure 3, examples of fixed values include contact and via sizes 7, transistor sizes 8, resistor sizes and capacitor sizes. Fixed geometry value examples are shown, where geometry dimensions must equal a defined value.

Finally, all integrated circuits are designed to have the co-ordinates of each shape as a multiple of a pre-defined grid. The scaling factor must take the new design grid into account and this can be accomplished in two ways, by calculating the scaling factor to ensure that the co-ordinates of all shapes in the scaled layout fall on the grid, or by snapping co-ordinates to the grid as they are scaled. All co-ordinates in the final chip must be place on the defined design grid

The scale factor for any process migration will be calculated from the ratio between the rules in the new manufacturing process specification and the rules used for the original device. There are three distinct parts of a chip that can be the limiting factor in scaling the design and the ratio of each must be calculated. The largest of the three ratios will be defined as the limiting factor in scaling the chip.

1. Interconnect scaling ratio.

The width and spacing for each routing layer must be calculated as a ratio defined by:-

Interconnect scaling ratio = (new width + new spacing) / (old width + old spacing)

Figure 4 shows interconnect spacing 10 and width 11.

2. Via size ratio and enclosure.

The via size is the size of the fixed rectangles that make up the via holes between routing layers:-

Via size ratio = Max ((new via 1 / old via 1), (new via 2 / old via 2), ...)

Figure 5 shows a via geometry 12 that includes a first layer 13, a via 14 and a second layer 15, and a 3x2 array 16 of via geometry.

3. Transistor geometry ratio.

The transistor geometry ratio is the relative shrink of the shapes that make up the distance between two transistors in separate pieces of diffusion:

Transistor geometry ratio = New (2a + 2b + 2c + 2d + e)/Old (2a + 2b + 2c + 2d + e)

Figures 6a and 6b show various CMOS transistor geometries, where L = transistor length and W = transistor width.

The maximum value derived from these calculations will determine the scaling factor. This scaling factor is rounded up to the next whole grid point, i.e. mod (scale grid) = 0.

A fourth factor that may need consideration concerns circuits that contain resistors and capacitors. These need to be scaled depending on the values of the materials used to construct them in the two manufacturing processes. Resistors and capacitors are defined by the value per square unit of the materials used in their construction. The ratio of these values in the old and new manufacturing process is used to calculate the scaling factor for these circuit components. This is described in more detail below with reference to Figs. 23 and 24.

Once the scaling factor has been determined, it is applied to each cell and geometry in the whole chip. Each co-ordinate is multiplied by the scaling factor to reduce the chip in size while keeping the geometries and hierarchy of the chip intact. At this stage, the new chip will be identical to the old in everything but scale.

The scaling of geometries and cells may be defined as coordinate scaling. Each scalar value is adjusted by:-.

(x co-ord * scale) (y co-ord * scale)

Figures 7a and 7b show general scaling. In the general scaling process, the original chip 18a is scaled down to create the new chip 18b, and each shape 19a,19b,19c in the original chip is replaced by a scaled down shape 20a,20b,20c. In each case, the new dimensions are equal to the old dimensions multiplied by the scaling factor. Each shape within the layout will be adjusted relative to the origin of the chip's axis, i.e. $x = 0$ $y = 0$.

The CMOS transistors in a circuit are determined by the overlap of two materials, doped silicon, known as diffusion, and polysilicon or occasionally metal. When scaling the width and length of a transistor, it is not always possible to apply an absolute value to every diffusion and polysilicon shape through the layout. Instead, the diffusion and polysilicon that make up the width and length of the transistor must change by a percentage of the transistor size and so each one must be scaled in turn and adjusted as a multiple of its current size. This involves the use of an edge adjusting method that identifies the edges of diffusion and polysilicon that make up each transistor's width and length and moving them to meet the required component value. Edge adjustment can be considered as distinct from scaling. Figure 8 shows a CMOS transistor definition and value definition.

The individual transistors are identified with a Boolean operation that places a marker shape over any area where polysilicon 21 crosses diffusion 22. These shapes will form the basis for the rest of the transistor sizing operations in a circuit containing CMOS transistors.

The diffusion and polysilicon edges that make up the transistor are selected and moved by a percentage of the gate width or length to adjust the value of the transistor. One piece of diffusion may make up several transistors so the scaling routine must process each edge in turn to achieve the correct value for all of its transistors. Figures 8 and 9 show CMOS transistor edge adjustment.

As shown in Fig. 8, the gate length L of a transistor can be altered by adjusting the edges 23 of the polysilicon 21 forming the gate. The width W is adjusted by moving the edges 24 of the diffusion 22 across the polysilicon 21. By adjusting these edges 23 and 24, the parameters of the transistor can be altered, thus changing their effect on the overall circuit.

As shown in Fig. 9, many transistors may be constructed out of one piece of diffusion material 25, and adjusting the edges that make up one transistor may therefore have an effect on the others. By examining each edge on the diffusion, adjustments may be made that ensure all transistors meet required parameters. If necessary, an edge making up more than one transistor may be split to accommodate the required device sizes. For example, the edges 26 and 27 may be split at the points marked "X" to make the changes correctly.

Some manufacturing processes may require transistor sizes to change by a differing amount, depending on their original size or function in the circuit, so a method of defining them such as an equivalence table may be used to adjust the scaling process to meet these restrictions.

Once the entire layout has been scaled, each layer that makes up the design must be grown or shrunk to meet the design rules of the new manufacturing process. This is achieved with a technique called hierarchical layer scaling, which can grow or shrink the shapes in the circuit while maintaining connectivity between cells.

All of the shapes on a layer may be merged together with a Boolean function before scaling to remove excess overlaps between shapes and maintain connections between shapes on the same layer. In order to maintain the electrical integrity of the circuit, the connections between shapes on the various layers must be maintained, even if these shapes occur at a different level in the hierarchy. If they become separated, the circuit will not function so it is essential that the layer scaler takes this into account.

The problems of layer connectivity only occur when the layer in question is to be shrunk and the data contains hierarchy. By moving all of the edges of a shape inwards, they will detach from the shapes in sub-cells and this will break the electrical connectivity in the circuit.

Figure 10 is illustrative of layer shrinking breaking connectivity. The circuit includes a top cell 30 and a number of sub-cells 31a,31b,31c. A shape 32a in the sub-cell 31a abuts shapes 32 in the top cell. If all the shapes 32a,32b,32c shrink they will become detached from each other, as shown in Fig. 10d.

In order to remedy this, the shapes in the sub-cells are copied to the top level and merged with the data at that level before the shrink is applied. Once the shrinking process is complete, the shapes from the sub-cells are applied as a template to remove any excess material.

It is also possible to hold layer data to the edge of a cell which is defined by the bounding box of the cell's data or by a shape representing the boundary. Layout data may be held on the boundary of the cell to preserve scaling connectivity.

Figure 11 illustrates hierarchical layer shrink with connectivity. In the example all three shapes 32a,32b,32c shrink but they retain the connection between them. Only the non-connected edges are shrunk. Further rules may be applied to the layer scale to restrict its operation to shapes that match given size rules, i.e. they are less than or greater than a given dimension. This allows data on the same layer to be scaled by differing amounts.

Figure 12 shows layer sizing by geometry width, the original shape 33a being replaced by the modified shape 33b. In this example, segments 34a,34b,34c of the shape can be shrunk if they meet size criteria. The shrunk segments 34a,34c stay attached to the large segment 35.

In order to meet all of the design rules for the migrated chip, it is necessary to make adjustments to parts of the shapes that make up the chip rather than the shapes as a whole. This can be described as "polygon edge adjustment", which examines each vertex of a shape and adjusts it according to its position relative to other shapes in the layout.

The edges to be adjusted may be defined by the shapes on an individual layer or identified for modification by Boolean logic to define their function in the circuit. Once this has been determined, the edges can be adjusted by an absolute value from their current position or relative to another edge on the same or a different layer. They may also be adjusted by a percentage of their distance to another edge on the same or different layer. Figure 13 shows edge adjustment for transistors. It is possible to adjust a first edge 36 that defines the transistor, or a second edge 37 for minimum overlap of transistors or contacts.

Integrated circuit layouts use contact and via holes in dielectric layers to allow routing layers to connect the circuit's components. These are typically square shapes with a size and spacing defined in the technology's design rules. Connections between wide tracks of material require bigger contact areas. This may be defined by one big contact or, more usually, as an array of uniform contact shapes.

Contact and via shapes may be scaled as above. Alternatively, the existing contacts and vias may be removed and replaced with arrays of new shapes conforming to the new design rules. These may either be cells that make up the contact as a single array of shapes or a series of rectangles that cover the area to be connected. This area is defined through a sequence of Boolean functions that isolate the area to be connected. The new shapes conform to the new design rules by construction rather than scaling.

Contacts between other materials such as metal and polysilicon may be updated using the same techniques. As shown in Figs. 14a and 14b, contacts and vias 40 are used to join the silicon 41 in the components to the metal wires 42 that connect the circuit. They are also used to connect different layers of metal together to allow for complex wiring. Most integrated circuits will have multiple layers of wiring connecting the components. These contacts and vias are actually holes in the dielectric material 43 that separates the different layers from each other.

Contact shapes from metal to silicon are often created as simple polygons rather than instances and each of these is replaced with a new shape that meets the new design rules. Each contact is removed and replaced with a new shape that has the correct dimensions.

In many cases, it is preferable to add as many contacts as possible between layers to help reduce current density through each contact. This can be achieved by identifying the area containing the contacts through a series of Boolean functions, and this area can be filled with as many contacts as will fit. For example, as shown in Figs 15a and 15b, the two large contact holes 44 of the old technology placed where the metal 42 overlaps the silicon 41 can be replaced in the new technology by eight smaller contact holes 45.

Certain layers in an integrated circuit's layout are required to overlap other layers by an amount defined in the design rules. These layers are forced to comply with the design rules through Boolean logic or through edge adjustment as defined above.

Common examples of layer overlap include polysilicon overlap of gate and metal overlap of contact. Figure 16 shows layer overlap. The polysilicon 48 must overlap the diffusion 49 by a minimum fixed distance 50.

Variations between integrated circuit manufacturing processes may mean that some layers in the original chip need to be removed and others added. Examples of this would be implant layers or isolation wells.

All shapes on superfluous layers are removed hierarchically, by identifying each shape on that layer and deleting it.

New layers may be defined in relation to an existing layer, possibly in conjunction with another layer: e.g. by placing a well around a diffusion layer, but only if it is crossed by polysilicon and makes a transistor. For example, figure 17a shows a diffusion 52 in a transistor 53 and a diffusion 54 outside the transistor. As shown in figure 17b, a new layer 55 in only added around the diffusion that is part of the transistor 53.

Data can also be promoted to new layers such as extra routing layers. Routing information may be promoted from an existing layer up to a new layer. This will allow the layout to be compressed to take advantage of gaps created when these shapes are moved. Figures 18a and 18b show moving routing data between layers. In the old arrangement shown in Fig. 18a, a first metal routing 56 is connected to a second metal routing 57 through a metal1-metal2 via 58. In the new arrangement shown in Fig. 18b, routing information from a first metal routing 56 promoted to a third metal routing 59 and the vias 58a are changed accordingly.

Figures 19a and 19b show swapping new via cells for old. The via cell 60a defined by the old technology contains shapes for connecting two metal layers, first metal 61 and second metal 62. This is swoped for a new via cell 60b containing shapes for connecting the metal layers in the new technology. Most vias are placed as instances of a sub-cell that

contains the three shapes that are used to construct it: two metal layers and a via layer. These can simply be replaced with a new via cell containing the same three layers, or re-sized to the new design rules. Some vias may be larger than minimum size and have multiple via holes connecting the two metal layers. When swapping these for a new via cell, the new cell is sized to match the number of via shapes in the old. By swapping each via cell in this way, the vias in the circuit are updated to meet the constraints of a new technology.

Once the entire circuit or a portion thereof has been migrated, it is verified using industry standard design tools. These will include a design rule checking (DRC) system and a layout-versus-schematic system (LVS). These will ensure that the newly migrated chip conforms to the new design rules and has retained the integrity of the connections within the circuit.

In addition, an interconnect timing analyser may be applied at any time to check the layout will perform correctly in the new manufacturing process. This may be applied after general scaling as a rough guide to the circuit's performance in the new process, even though it does not conform to the new design rules. A more accurate simulation will be available once the migration process is complete.

When the layout migration is completed and the new chip has passed verification, it may be delivered in an industry standard format such as GDSII or CIF.

The steps of the migration process will now be described with reference to the flow diagram shown in Fig. 20.

The first step 70 is to input the original data. The original data is supplied in an industry standard format such as GDSII or CIF. The database will contain the shapes that make up the layout of the circuit and will include circuit elements such as rectangles, polygons, paths, instances, arrays and text. Connectivity information may also be contained in the database but the migration tools do not need this information to function.

The second step 71 is to analyse and clean the data. The time taken to migrate the data may be improved by modifying some of the data before starting the main migration

routines. This could include merging separate overlapping shapes or converting interconnect elements from polygons to paths. Changes in the hierarchy of the circuit may also be useful such as converting individual shapes that make up a connection between layers to an instance of a connection cell.

While these techniques may improve the migration process, they are not necessary to complete the migration process.

The third step 72 is to calculate the scale factors. The scaling factor in a process migration will be determined by the ratios of the rules of the old manufacturing process and the rules in the new one. Examples of these rules are given above.

The fourth step 73 is to save the device data. Information contained in the original database may be referenced by programs throughout the migration process and so it is useful to be able to refer to this data easily. One technique, which is described in more detail below with reference to Fig. 22, is to add a node containing design parameters to each device in the layout. These nodes can be used to store information about the devices such as sizes or names of drawing layers.

The fifth step 74 is to scale the design. Once the scaling factor is decided, each co-ordinate in the design is multiplied by that scaling factor, giving a design identical to the original in everything by size.

The data for each element is scaled as follows:

Rectangle:	Lower-left(X) * scale
	Lower-left(Y) * scale
	Upper-right(X) * scale
	Upper-right(Y) * scale
Polygon:	co-ordinates(X) * scale
	co-ordinates(Y) * scale
Path:	co-ordinates(X) * scale

co-ordinates(Y) * scale
width * scale

Text: co-ordinate(X) * scale
co-ordinate(Y) * scale
font size * scale

Instance: co-ordinate(X) * scale
co-ordinate(Y) * scale
magnification * scale

Array: co-ordinate(X) * scale
co-ordinate(Y) * scale
magnification * scale
delta(X) * scale
delta(Y) * scale

The sixth step 75 is to size the layers. Once the data is scaled, each layer may be sized to meet the minimum width value defined in the design rules. This may be done to ensure that the data on each layers meets the rule for spacing and also has the advantage of reducing capacitance on each layer and improving circuit performance. Overall scaling calculations may take a subsequent adjustment in a layer's size into account when deciding on the primary scaling factor for the design.

Layers may be scaled by an absolute value or by a percentage of the layers size. To scale a layer by an absolute value, the following calculations are applied:

Rectangle: Lower-left(X) + value
Lower-left(Y) + value
Upper-right(X) - value
Upper-right(Y) - value

Polygon:	co-ordinates(X) + or - scale*
	co-ordinates(Y) + or - scale
Path:	width * scale

*Addition or subtraction of the scale number will depend on the position of the co-ordinate on the hull of the shape. If it is on the a bottom or left edge of the shape, the scale number will be added to the co-ordinate, if it is on the top or right edge of the shape, it will be subtracted.

Relative scaling involves multiplying each co-ordinate in the shape by the same scale factor to adjust the co-ordinates.

The data for each element is scaled as follows:

Rectangle:	Lower-left(X) * scale
	Lower-left(Y) * scale
	Upper-right(X) * scale
	Upper-right(Y) * scale
Polygon:	co-ordinates(X) * scale
	co-ordinates(Y) * scale
Path:	co-ordinates(X) * scale
	co-ordinates(Y) * scale
	width * scale

This technique will resize the shapes but it will also offset them from their position relative to the rest of the shapes in the circuit. In order to return them to their original position, the centre point of each shape can be calculated and the new shaped moved back to the central position of the old. The centre point is defined by taking the middle of the rectangular convex hull of the shape.

The seventh step 76 is to size the CMOS transistors. The shapes that make up the transistors will be sized along with all of the other shapes in the layout when general scaling is performed. Further sizing may occur when individual layers are scaled when those layers are part of a transistor, i.e. diffusion or polysilicon. However, transistors may need to be scaled to account for other factors such as circuit timing and driving capabilities. The transistor scaling process is described in more detail above with reference to Figs. 8 and 9. In addition, the resistors and capacitors may also be adjusted, as described in more detail below with reference to Figs. 23 and 24.

The eighth step 77 is to update the contacts. This process is described in more detail above with reference to Fig. 15.

The ninth step 78 is to add and/or delete layers. Different manufacturing technologies may have a different number of layers making up the chip. Examples of this include implant and well layers.

These new layers are generated around existing layers and this can be achieved by copying each shape in the defining layers, oversizing it and then moving it onto the new layer. Any gaps between shapes on this new layer should be filled with the same material if they are found to be less than the specified minimum distance in the design rules.

If the old layout contains shapes that are not required for the new manufacturing process, each of these shapes can be deleted from the database.

The tenth step 79 is to check the design. Once the migration process has been completed, the design can be checked using standard layout verification methods. These include design rule checking (DRC) and layout verses schematic checking (LVS). It may also be useful to perform a comparison between the old and new layouts (LVL). All of these checking techniques are considered standard in the electronics industry and software to perform these checks is available from a variety of vendors.

Transistors are adjusted by altering the dimensions of the shapes that are used to construct them. This is true for bipolar (NPN & PNP) devices and MOS (field effect) devices. Bipolar transistors can usually be considered as discrete components but MOS devices

will often be combined to save space in the circuit. The scaling calculations for a bipolar device will be governed by the rules that make up that device, which will include minimum widths, spacings, overlaps and enclosures.

The ratio of each of these rules in the old and new design rule specifications must be accounted for in the scaling calculations. The sizes for a CMOS transistor are defined by the common region of polysilicon overlapping diffusion. The width and length of the overlap defines the value of the transistor and adjusting the edges of the two shapes alters its value.

The layer scaling process will now be described in more detail with reference to Fig. 21. In order to meet the specifications of the new design rules, individual layers may need to be scaled up or down after general scaling is complete. This will ensure that the data will meet the requirements of the new manufacturing process and metal connection layers are reduced to their minimum width to reduce capacitance in the circuit. Layer scaling is most often applied to interconnection layers and the diffusion and polysilicon layers that make up CMOS transistors.

The first step is to take the original data 81 and calculate the scaling factor 82. The scale factor for each layer is calculated after the general scaling factor has been applied and can be applied as an absolute value or as a percentage. These are calculated as:

Absolute value: $$\frac{(\text{old layer width} * \text{general scale}) - \text{new layer width}}{2}$$

Percentage value: $$\frac{\text{new layer width}}{\text{old layer width} * \text{general scale}}$$

The sizing value derived is taken from each side of a shape, hence the need to divide the value by 2.

It may be necessary to only alter the sizes of certain shapes while retaining others as they are. An example of this would be the wide power supply metal that is on the same layer as general interconnect shapes. In this case, only shapes that were narrower than a certain

value would be under or over sized. The process includes the steps of selecting the shapes 83 that should be scaled and applying the scaling factor 84 to that selection.

When the polygon shapes on a layer are undersized, they will become detached from each other thus breaking the electrical integrity of the circuit. This must be prevented to ensure that the circuit still functions after the sizing procedure. This is further complicated if the shapes attach to other shapes at different levels of the circuit's hierarchy as the problems of attachment will depend on where the shapes are placed. If the shapes in question are oversized, they will still overlap each other so this problem will not arise. The process includes the steps of selecting the undersized shapes 85 and selecting from those the shapes for which it is necessary to retain connections 86.

One method of keeping all of the shapes within a cell connected is to merge the shapes together before sizing them. This means that no connected shapes are discrete from each other and so will not become detached through the sizing process.

Connections between shapes at different levels of the hierarchy can be maintained by copying the original shapes to a temporary layer before under-sizing the data layer. Data on each sub-cell can be under-sized in turn while leaving the outline of the original in place. When layer data in a cell touches the temporary layer in a sub-cell, the connection can be maintained using a sequence of Boolean operations to select connecting shapes 87 and fill the gaps 88 between the top cell and sub-cell and maintain electrical integrity.

Once the size value and connectivity information has been defined, the shapes can be sized by an absolute value 89 or a percentage 90, followed by offsetting the shapes 91, as required.

A useful post processing function for layer sizing involves removing small notches 92 and bumps on each of the shapes on a layer that can be generated by the re-sizing programs. These should be removed as they are likely to result in errors being reported at the design rule checking stage.

A method for storing old design values in node properties will now be described with reference to Figs. 22a, 22b and 22c. Before the layout of the integrated circuit is

modified, it is useful to store the information about the current layout through some method for reference throughout the modification process. The information to be stored may include the sizes of the components that make up the circuit such as the widths and lengths of the transistors or the values of resistors and capacitors. By storing this information before modifying the design, subsequent modification routines can check their values against initial values without regard to how that data has been affected by the scaling process.

One method of storing this data is to save it to an ASCII file and use this for reference, but this has the disadvantage of being divorced from the database containing the layout and needs to have detailed information on the location of each component, making it overly verbose.

A better method involves storing this information with each component in the circuit. Interrogating these components will return the information derived from the original circuit for comparison with the components' new values. For example, the system may add a simple "node" object to the database which carries the information for the individual component. These nodes are unaffected by the scaling process and can carry the relevant information as properties.

For example, Figs. 22a, 22b and 22c show respectively a node placed over a CMOS transistor containing the original W/L values, a node placed over a resistor containing its type, dimensions and value, and a node placed over a capacitor containing its type, dimensions and value.

The resistor calculations will now be described in more detail with reference to Fig. 23. Resistors are created by placing a piece of semi-conducting material between two nodes. The two factors that define a resistor's values are the resistance required and the current to be drawn.

The resistance value of a resistor is governed by the ratio of its width W to its length L and the "sheet resistivity" of the material from which it is made. In the example shown in Fig. 24, the resistor has the following values:

P-diffusion resistor. Resistivity = 100 ohms per square.
Current density = 100 μA per square.
Value = 8.5 squares @ 100 ohms/square = 850 ohms
Current = 0.5 squares * 100 μA/square = 50 μA

When applying the scaling factor to resistors, these ratios of the sheet resistivity and current density of the old and new resistor materials have to be taken into account to obtain the same value in the new resistors. As both the width and the length of the resistor will be equally affected, scaling a resistor will result in an identical number of squares and, therefore, an identical value. However, the sheet resistivity of the new process may be different and this will need to be taken in to account to calculate its value. This is achieved using the equation:

*new number of squares = (old resistivity / new resistivity) * old number of squares.*

The width of the resistor after it has scaled will also affect the maximum current that the resistor can carry. The current involved will be dictated by the circuit around the resistor and so this value can only be obtained through examining circuit performance. If the resistor width needs to be increased to accommodate higher currents, the length must be scaled by an equal factor to maintain the same value of resistance.

The capacitor calculations will now be described in more detail with reference to Figs. 24a and 24b. Capacitors within an integrated circuit are formed by placing sheets of conducting or semi-conducting material 95,96 over one another with a third material 97 between them forming a dielectric. The types of layers that may be used are defined in the design rules for each manufacturing process and these will also specify the value of the capacitors as a number of Farads per square. As Farads are such large units, these will typically be defined in pico-farads or femto-farads.

The value of the capacitor is given by:

*width * length * nF per unit area*

As the value of a capacitor is almost entirely defined by its surface area, scaling a capacitor will always alter this value. If this is the case, the dimensions of the capacitor will need to be adjusted after the scaling process is complete to retain the value of the capacitor.

Claims

1. A method of modifying an integrated circuit, the method including the steps of:
   - selecting a scaling factor,
   - scaling the circuit according to the scaling factor, and
   - adjusting the circuit for functionality and design rule compliance.

2. A method according to claim 1, wherein the scaling factor is selected by calculating a plurality of predetermined scaling ratios and selecting a scaling factor that is equal to or greater than the largest of the predetermined scaling ratios.

3. A method according to claim 2, wherein the predetermined scaling ratios include the interconnect scaling ratio, the via size ratio and the electrical component geometry ratio.

4. A method according to claim 2 or claim 3, wherein the scaling factor is selected by rounding up to the next whole grid point from the largest of the predetermined scaling ratios.

5. A method according to any one of the preceding claims, wherein the step of scaling the circuit according to the scaling factor circuit includes multiplying the co-ordinates of the circuit geometry by the scaling factor.

6. A method according to any one of the preceding claims, wherein the step of adjusting the circuit for functionality and design rule compliance includes a hierarchical layer scaling process.

7. A method according to claim 6, wherein the hierarchical layer scaling process includes the step of scaling the components in a layer according to a predetermined layer scaling factor.

8. A method according to claim 7, wherein the hierarchical layer scaling process includes the step of scaling the components so as to maintain the connectivity of those components.

9. A method according to claim 7 or claim 8, wherein the hierarchical layer scaling process includes the step of identifying components that meet predetermined width criteria, and scaling only components that do not meet those criteria.

10. A method according to any one of the preceding claims, wherein the step of adjusting the circuit for functionality and design rule compliance includes a transistor edge adjustment process.

11. A method according to claim 10, wherein the transistor edge adjustment process includes the step of adjusting the width of the polysilicon layer and/or the length of the diffusion layer.

12. A method according to any one of the preceding claims, including the step of updating the contacts and vias.

13. A method according to claim 12, wherein the step of updating the contacts and vias includes removing the existing contacts and vias and replacing them with new contacts and vias.

14. A method according to any one of the preceding claims, including the step of adding and/or deleting layers.

15. A method according to any one of the preceding claims, including the step of checking the circuit using a layout verification process.

16. A method according to any one of the preceding claims, including the preliminary step of analysing and modifying the circuit data.

17. A method according to any one of the preceding claims, including the step of adding a node containing design parameters to devices in the circuit.

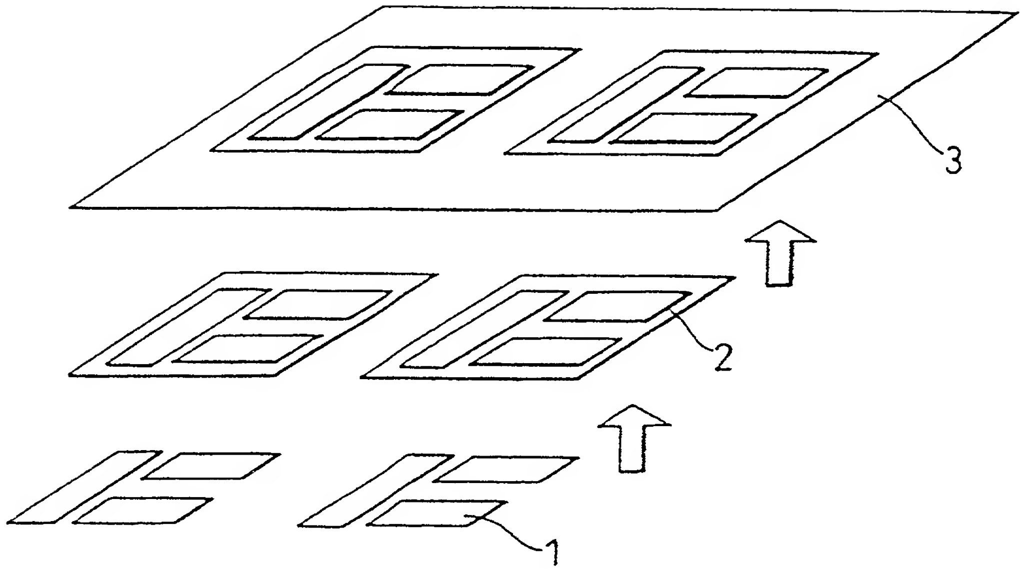


Fig. 1

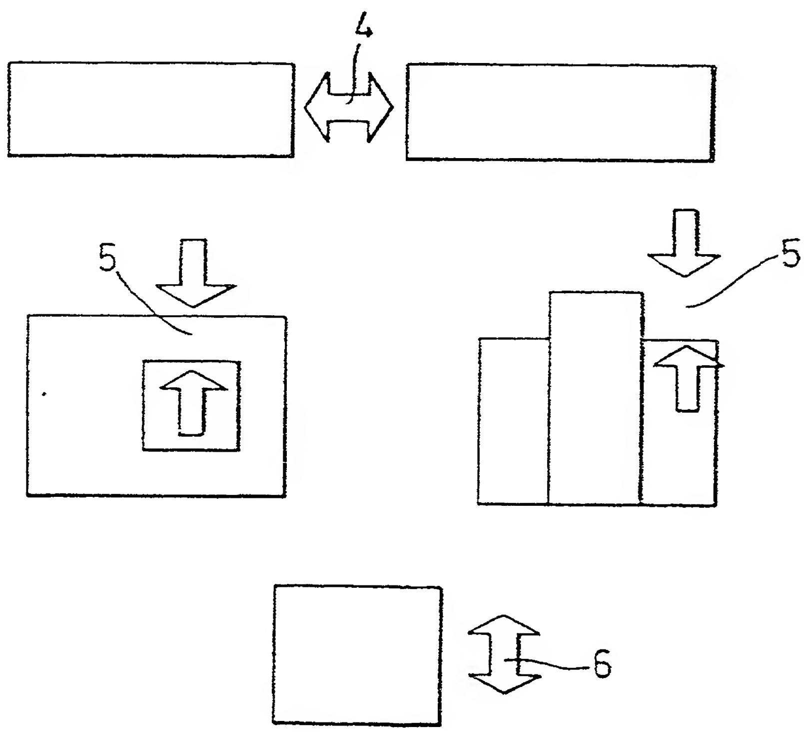


Fig. 2

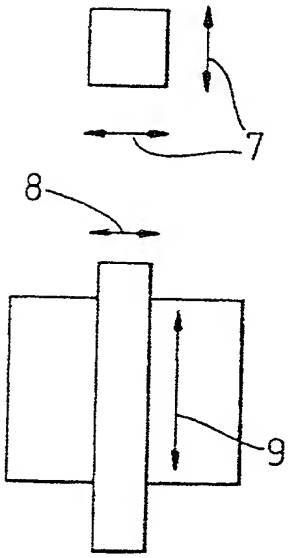


Fig. 3

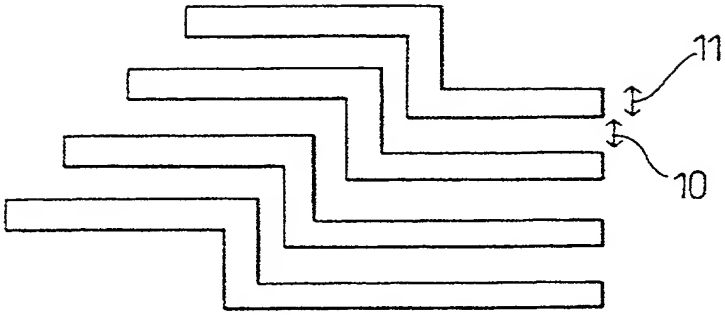
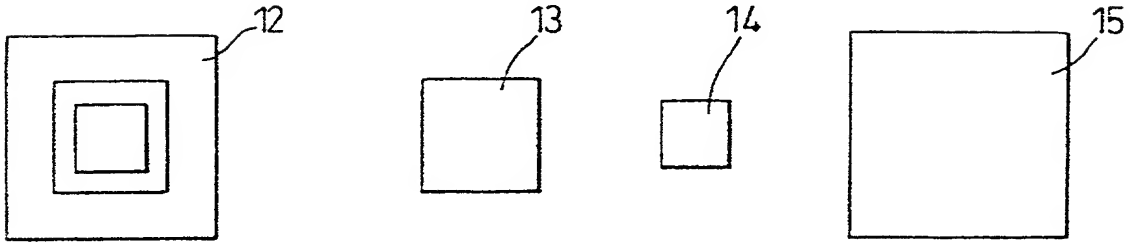


Fig. 4



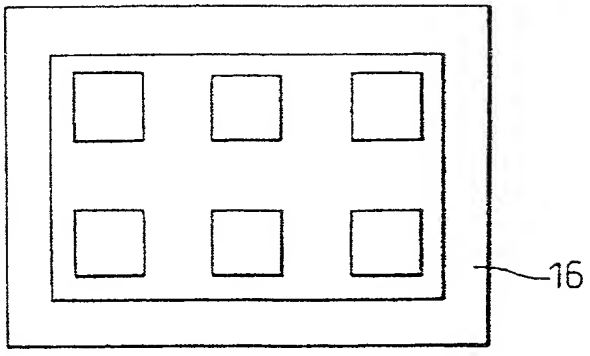


Fig. 5

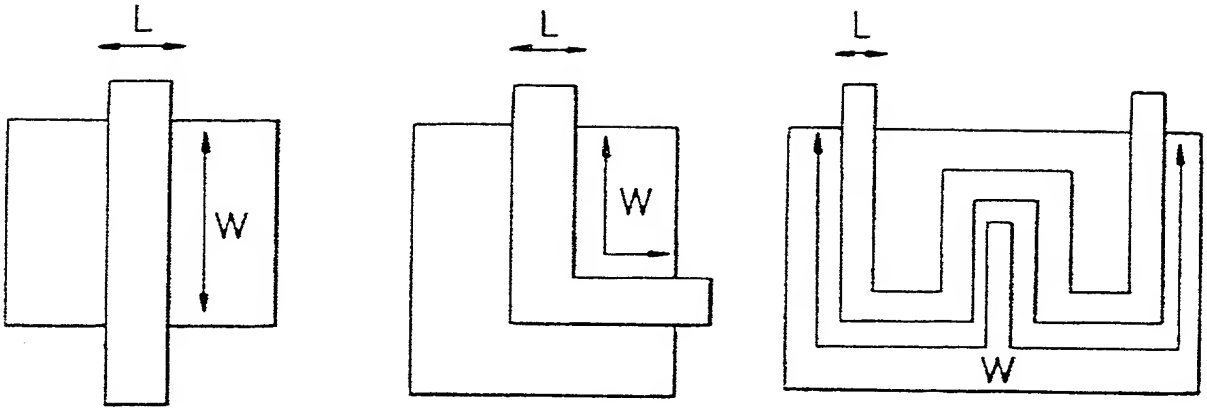


Fig. 6a

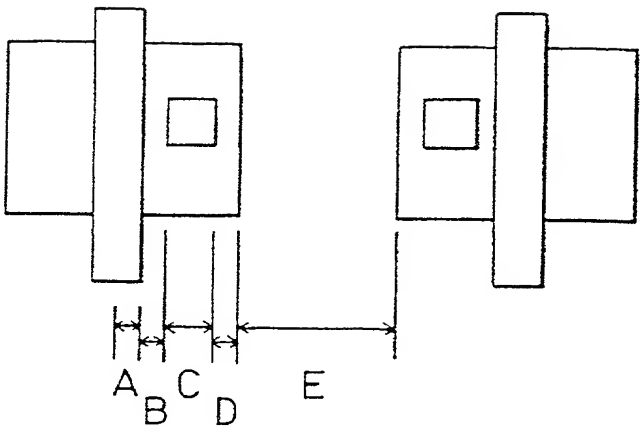


Fig. 6b

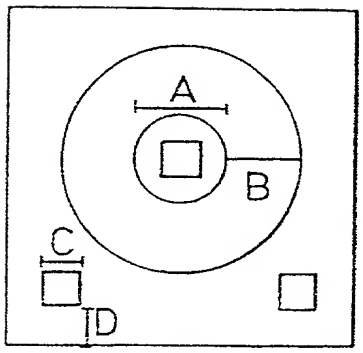


Fig. 6c

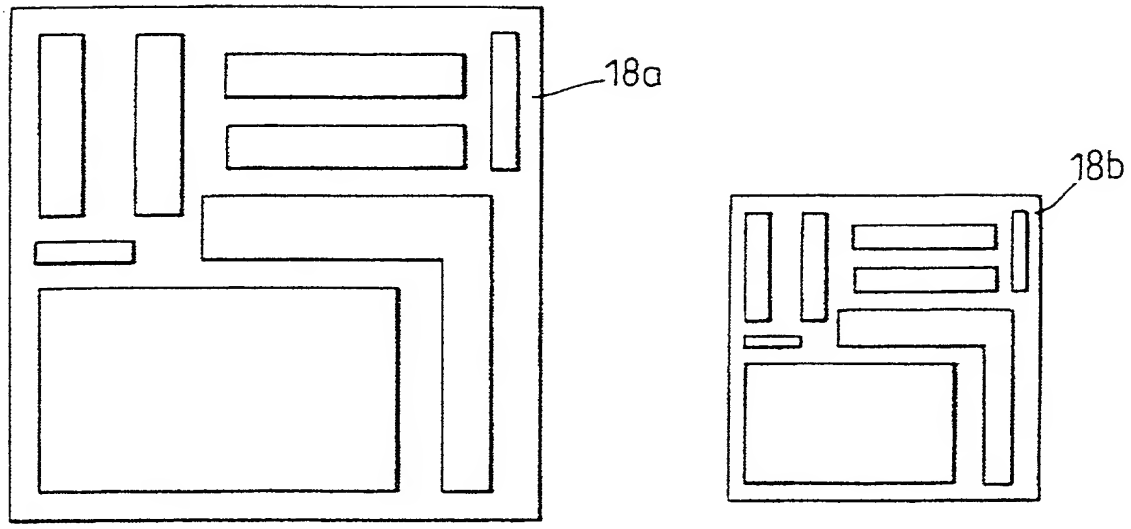


Fig. 7a

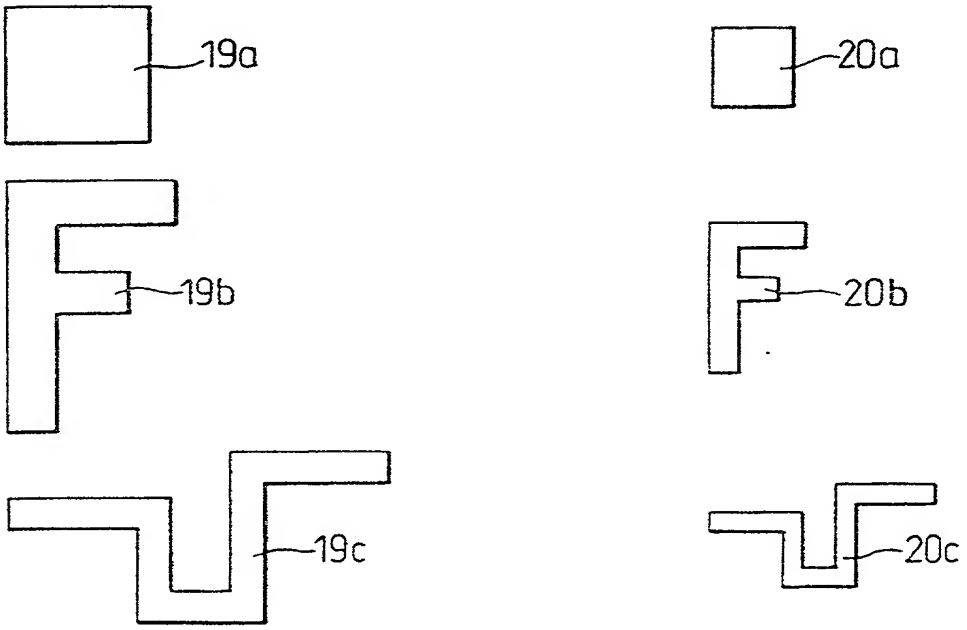


Fig. 7b

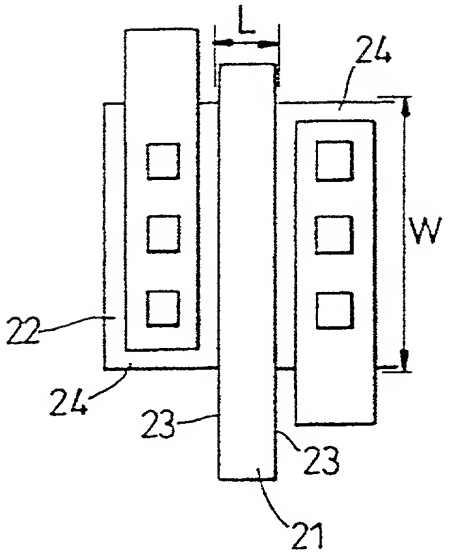


Fig. 8

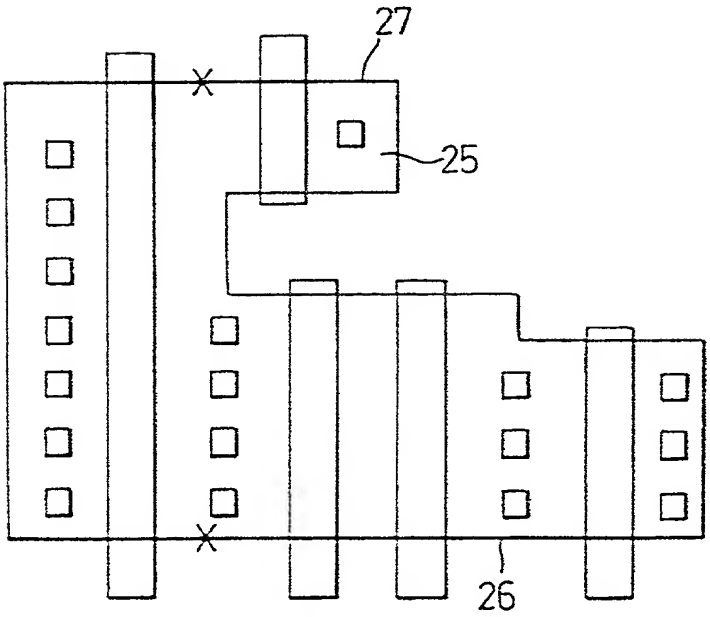


Fig. 9

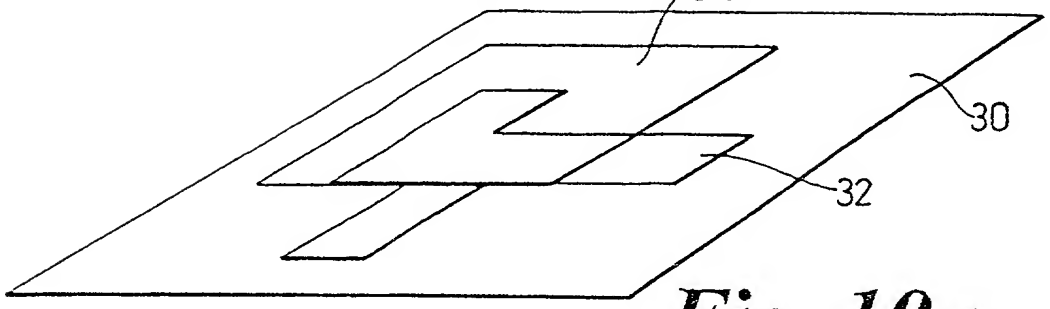


Fig. 10a

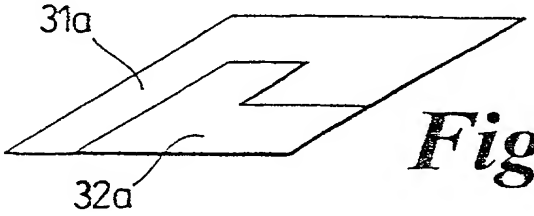


Fig. 10b

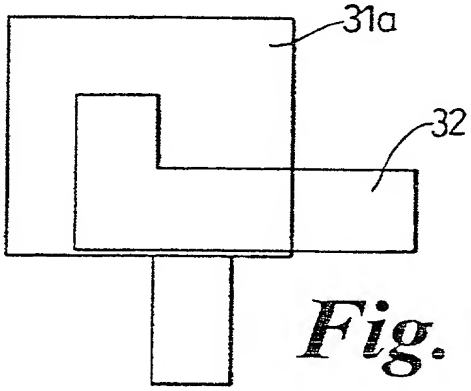


Fig. 10c

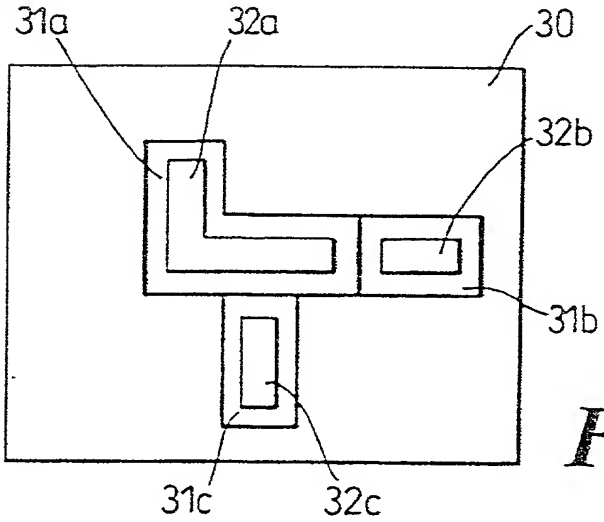


Fig. 10d

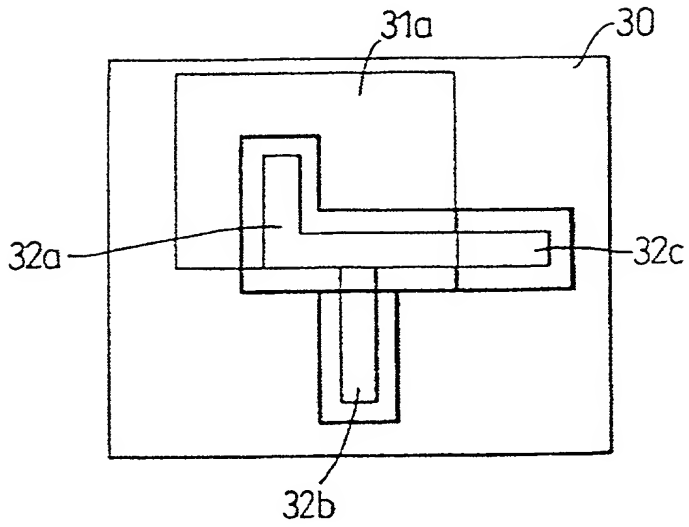


Fig. 11

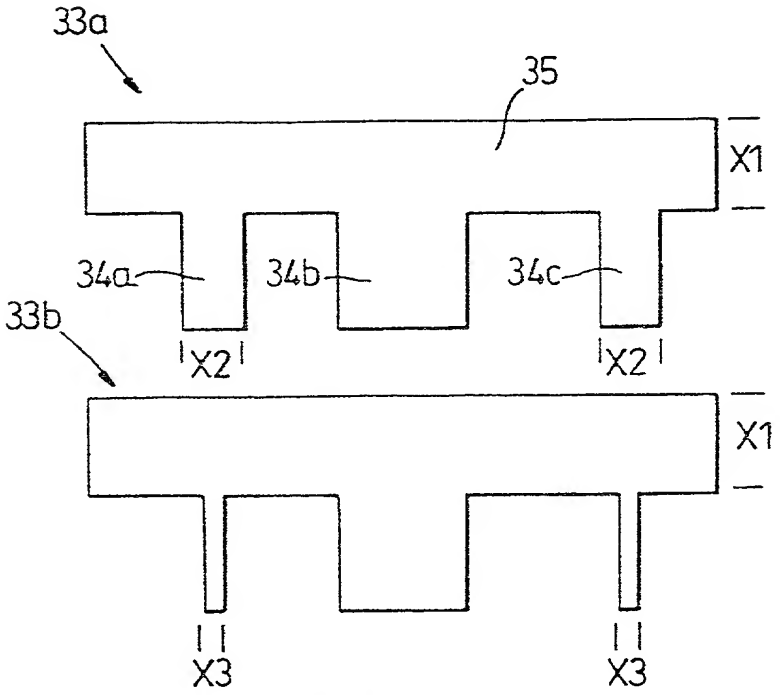


Fig. 12

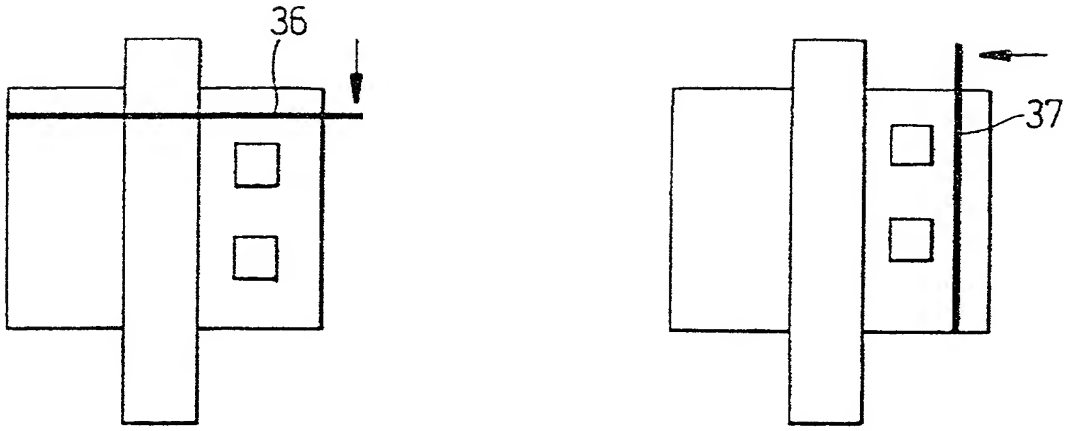


Fig. 13

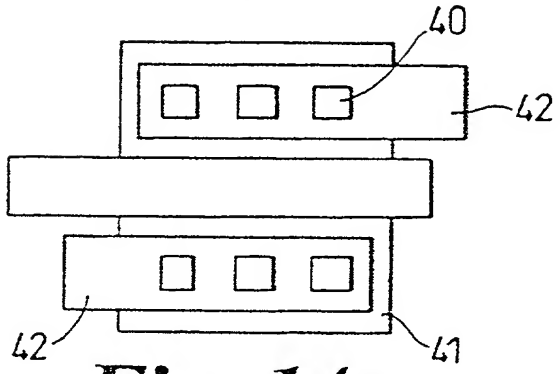


Fig. 14a

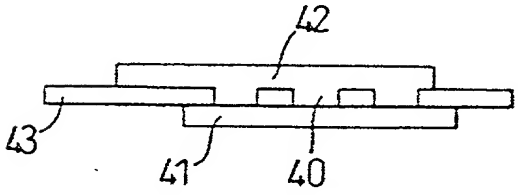


Fig. 14b

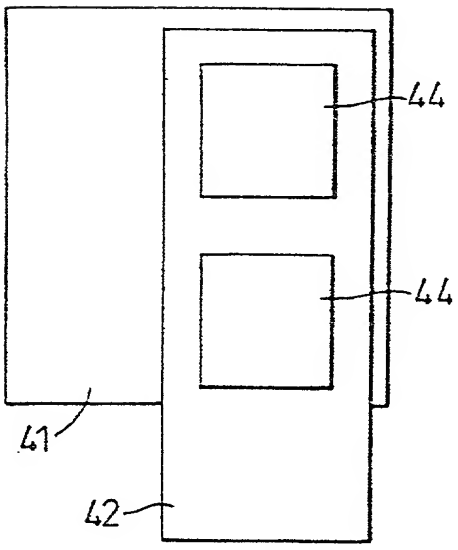


Fig. 15a

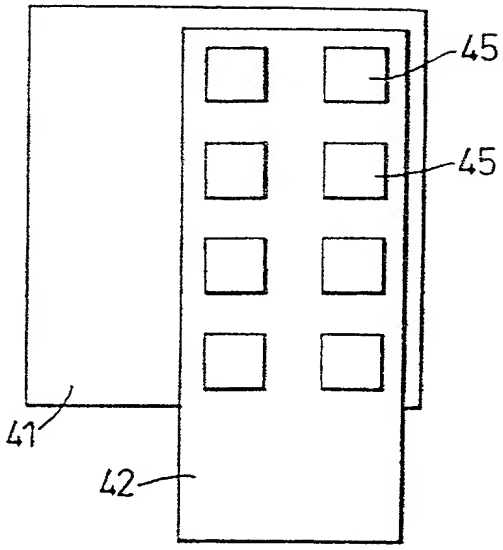


Fig. 15b

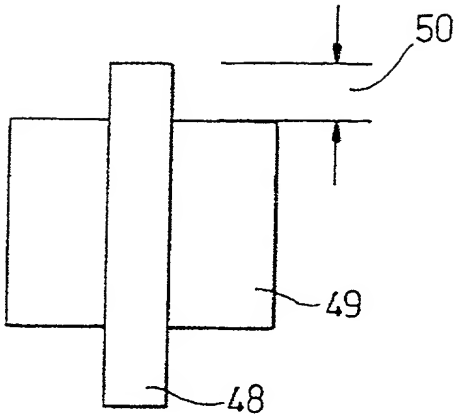


Fig. 16

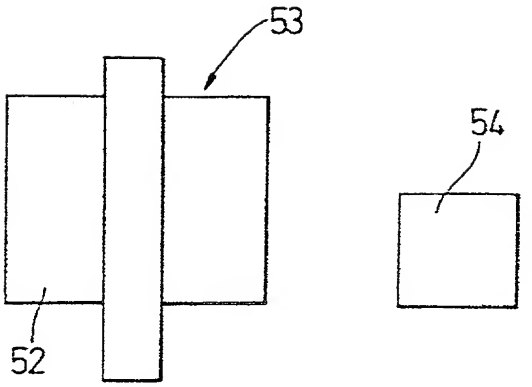


Fig. 17a

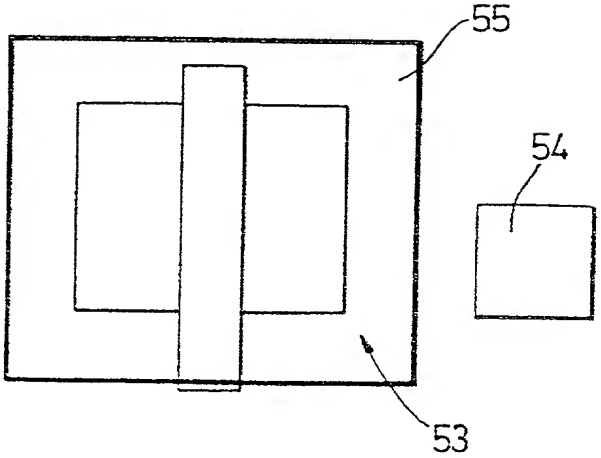


Fig. 17b

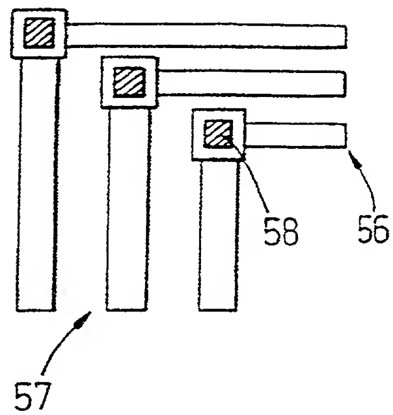


Fig. 18a

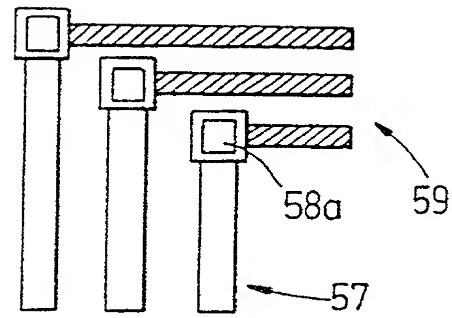


Fig. 18b

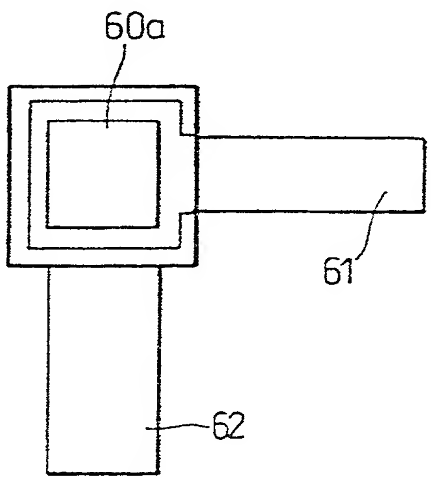


Fig. 19a

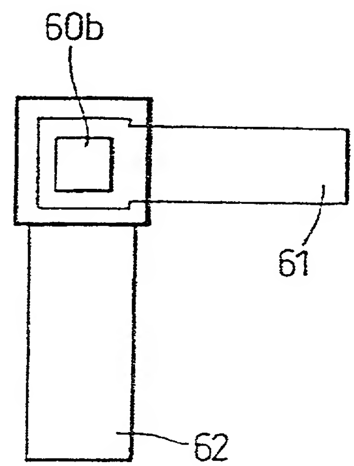


Fig. 19b

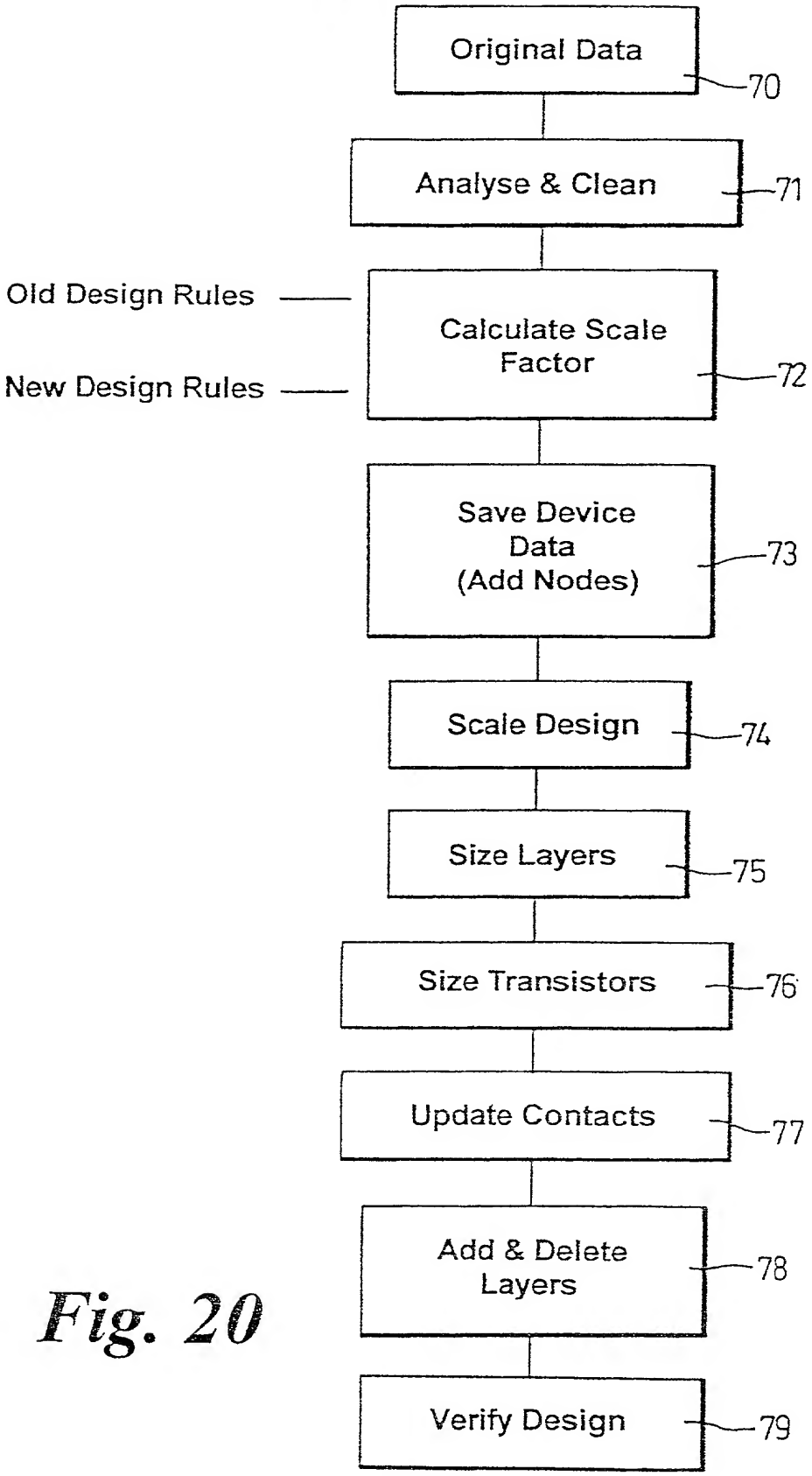


Fig. 20

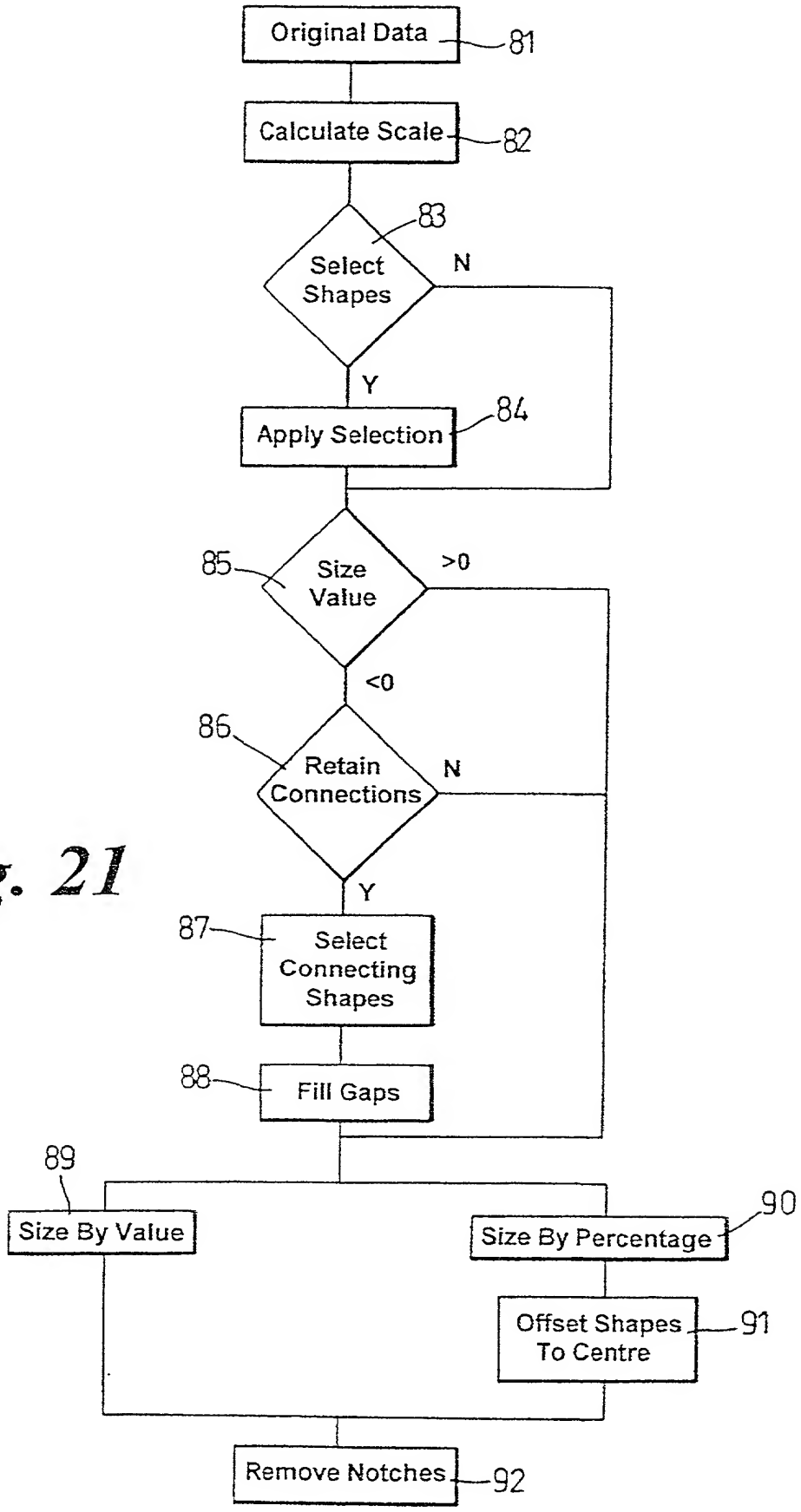

Original Data
81
Calculate Scale
82
83
Select Shapes
N
Y
Apply Selection
84
85
Size Value
>0
<0
86
Retain Connections
N
Y
87
Select Connecting Shapes
88
Fill Gaps
89
Size By Value
90
Size By Percentage
Offset Shapes To Centre
91
Remove Notches
92

Fig. 21

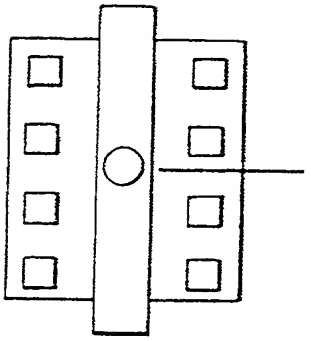


Fig. 22a

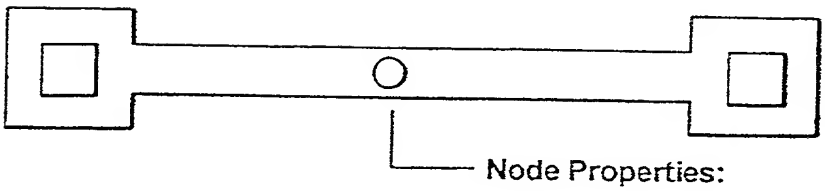


Fig. 22b

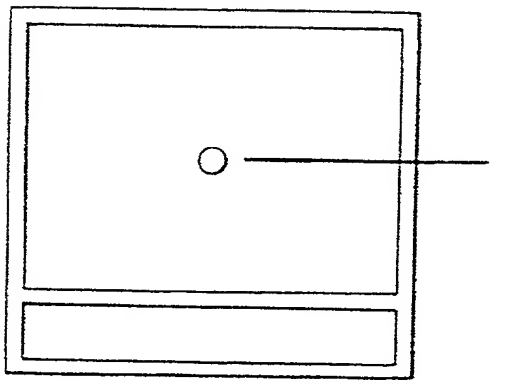


Fig. 22c

17/17

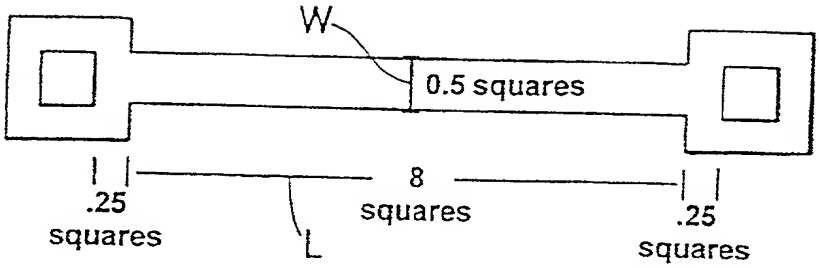


Fig. 23

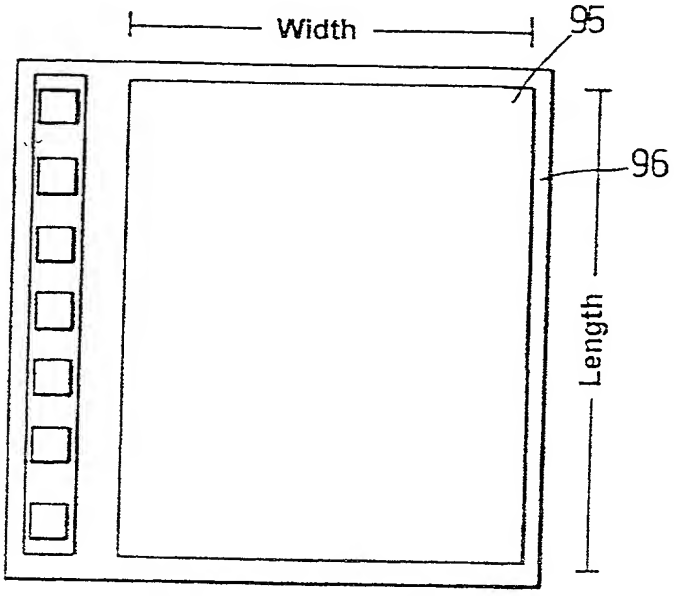


Fig. 24a

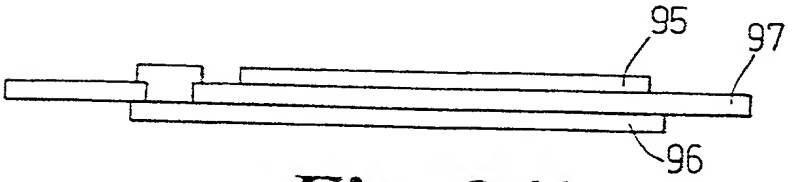


Fig. 24b

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket No. UDL 2 0016

As a below inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought by patent application filed on the invention entitled:

METHOD OF MODIFYING AN INTEGRATED CIRCUIT

the specification of which was filed on **December 19, 2001** having **Application Serial No. 10/018,867**, said patent application having been amended on December 19, 2001, and

said patent application having ***international application no. PCT/GB00/02256***, an ***international filing date of 21 June 2000*** and having been transmitted by the International Bureau of WIPO to the United States Patent and Trademark Office as a Designated Office on 28 December 2000 as noted on form PCT/IB/308.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to the patentability of this application in accordance with Title 37, code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119 or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application(s) for patent or inventor's certificate or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

9914380.2	Great Britain	21 June 1999
(Number)	**(Country)**	**(Filing Date)**

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Prior Provisional U.S. Patent Application(s):

(Application Serial No.)	(Filing Date)

I hereby claim the benefit under Title 35, United States, Section 120 of any United States application(s) or any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information which is material to patentability as defined in Title 37, of Federal Regulations Code, Section 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Application(s) or PCT Application(s) Designating the United States:

PCT/GB00/02256	**21 JUNE 2000**	
(Application Serial No.)	**(Filing Date)**	**(Status)**

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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